

# Model Name:MRHM7AP-LF

Revision 1.0

SHEET

TITLE

01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	PWRGD&RESET MAP
05	POWER DELIVERY CHART
06	CPU_1-PCIE_DMI_FDI_eDP
07	CPU_2-MEM Controller
08	DDRIII CHANNEL A,B
09	CPU_3-PWR
10	CPU_4-GND
11	HDMI,mDP
12	NM70_FDI, DMI,USB,PCI
13	NM70_DISPLAY,GPIO
14	NM70_HOST,SATA,HDA,SPI
15	NM70_CLK BUFFER,PCIE
16	NM70_PWR
17	NM70_GND
18	SIO ITE8773 , FAN,FP
19	AUDIO CODEC ALC887
20	AUDIO JACK
21	RTL8111E-CG/RTL8105E-H
22	LINNER POWER-1
23	DISCRETE POWER
24	AD19V & VCC5 & VCC3
25	VCORE & VCPU_VAXG NCP6131
26	
27	



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Title			
Cover Sheet			
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## D

C



B

A

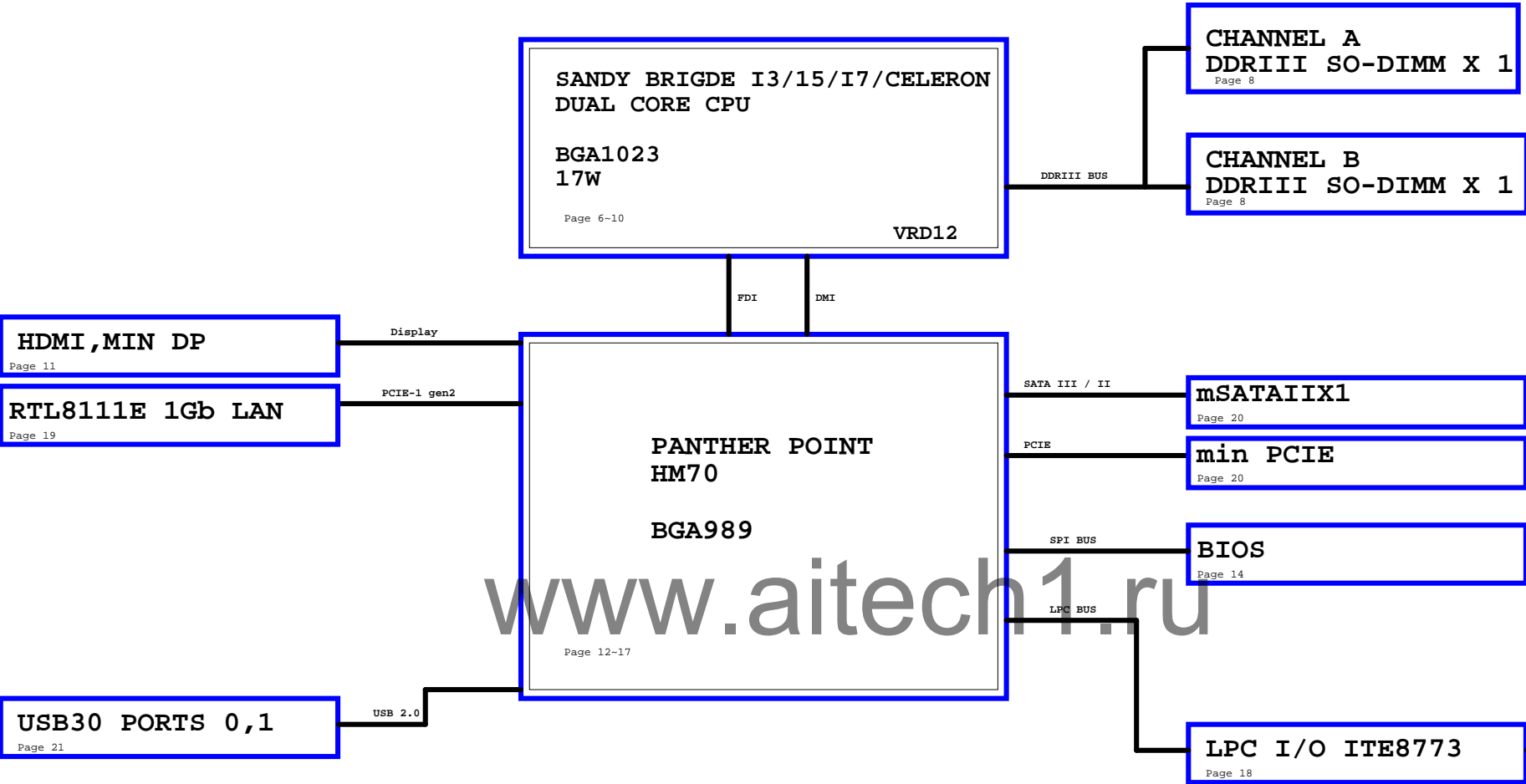
D

C

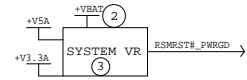
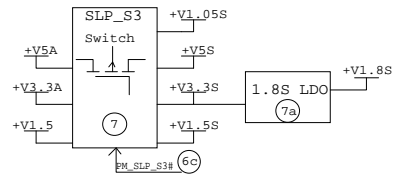
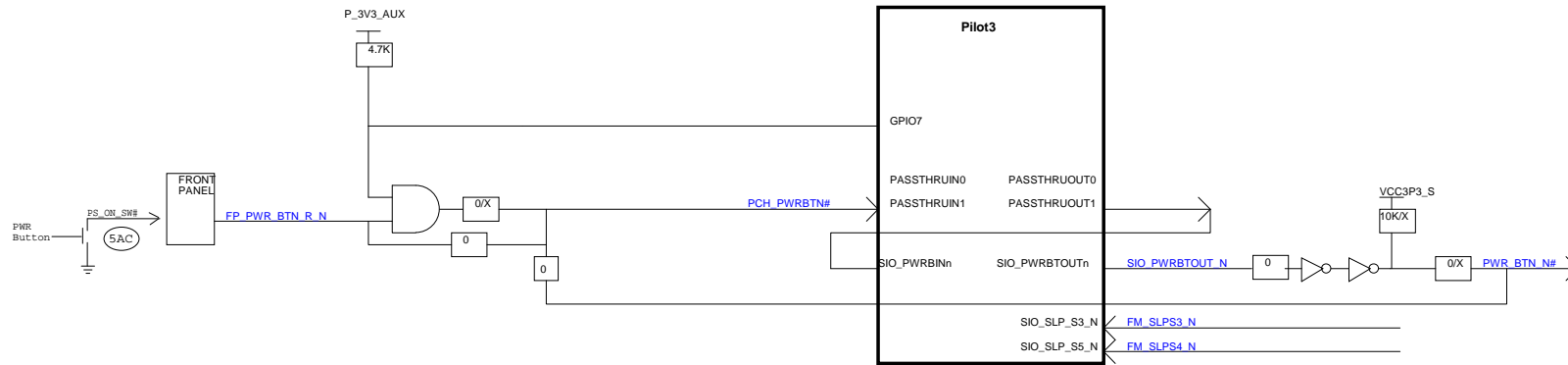
B

A

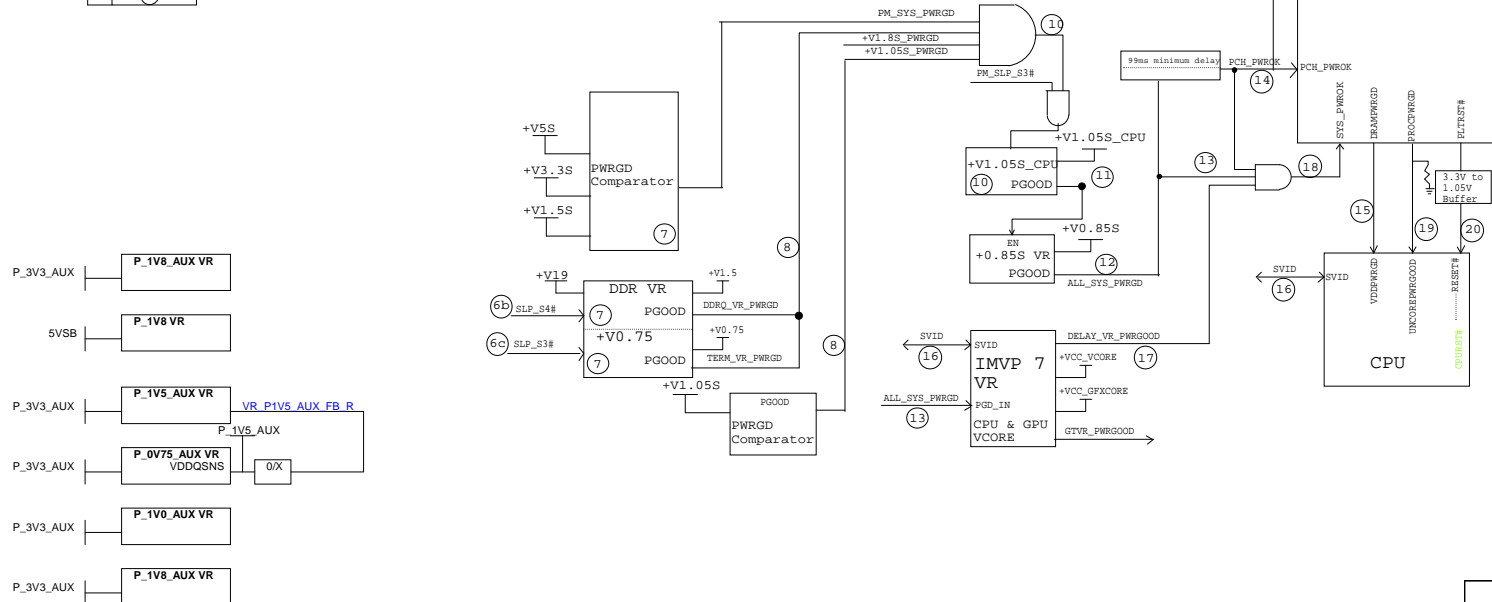
BLOCK DIAGRAM



# Huron River Power Up Sequence Diagram



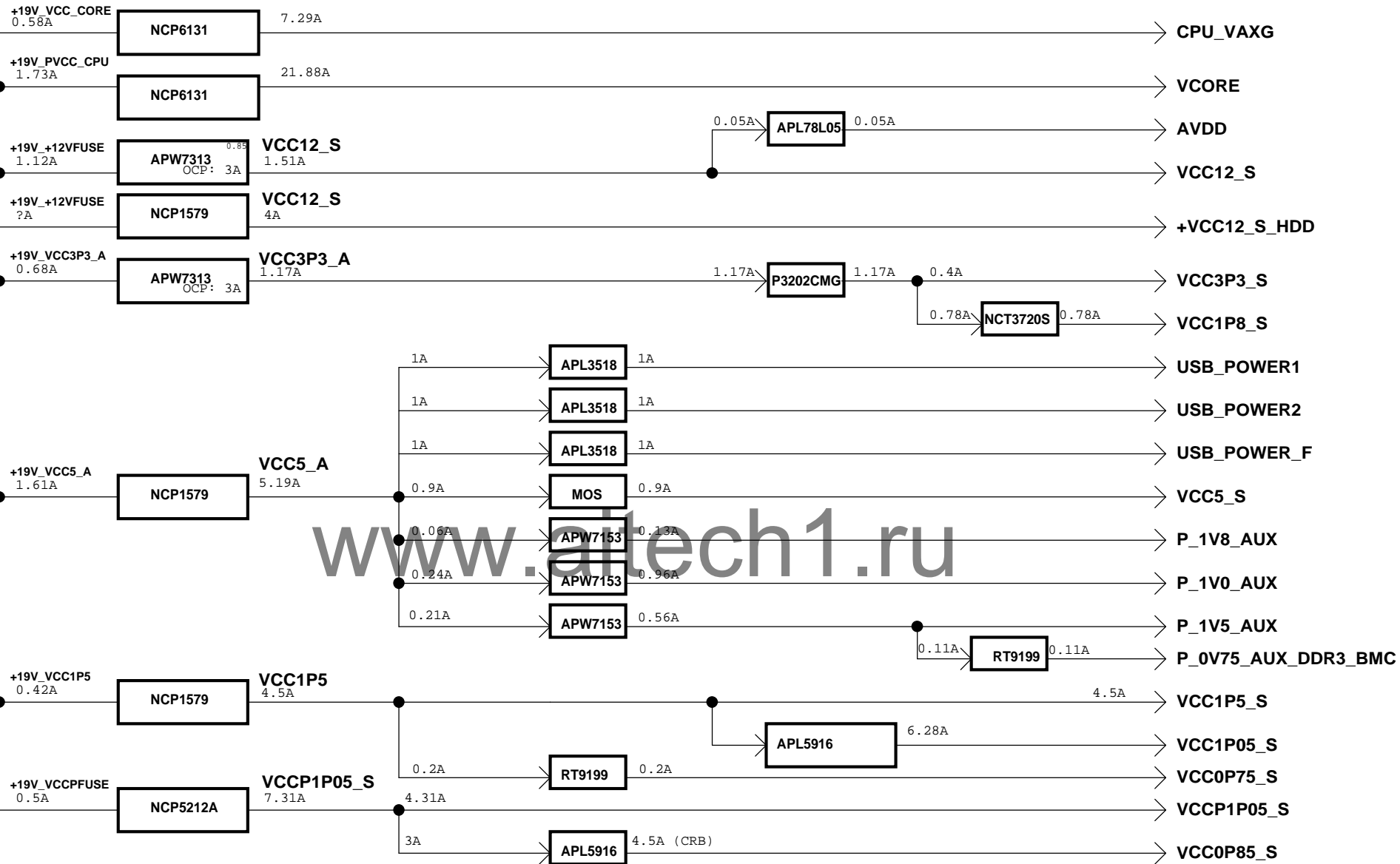
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PWRGD&RESET MAP			
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Adapter in

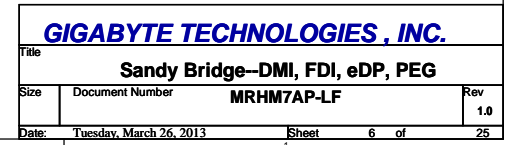
VBATA  
6.04A



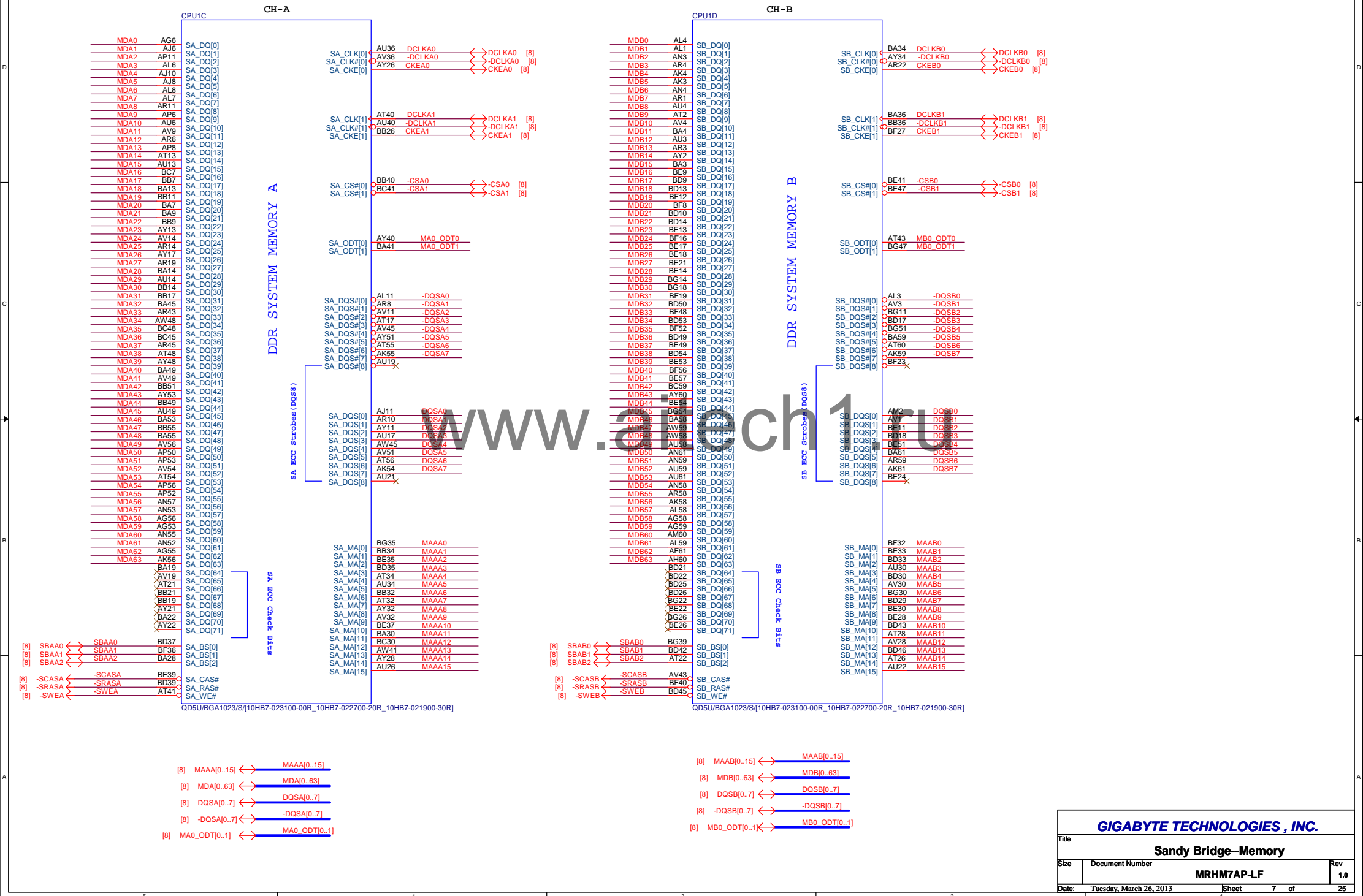
Title				POWER DELIVERY CHART	
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### ***Sandy Bridge 2C BGA Processor (CLK,MISC,JTAG)***

PEG\_ICOMPO 12 mils



Sandy Bridge 2C BGA Processor (DDR3)



# DDR Signal impedance

Signal Group	Signal	Impedance	Space to Others	Ref. Plane
Clocks	CLK	72 Ohm	7 H	VDDIO
Address	AD[0:15]	40 Ohm	2.5 H	VDDIO
Command	CMD[0:7]	40 Ohm	2.5 H	VDDIO
Control	CS[0:1]	40 Ohm	2.5 H	VDDIO
Data	D[0:31]	40 Ohm	2.5 H	VDDIO
Misc.	Other	40 Ohm	2.5 H	VDDIO or VSS

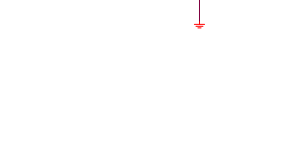
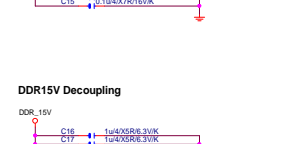
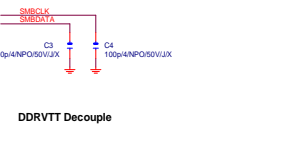
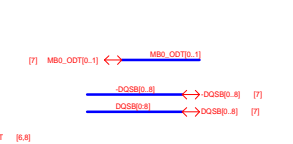
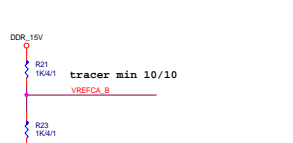
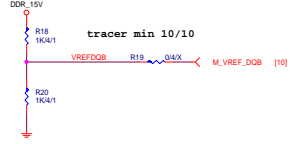
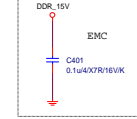
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## DDR3 SDRAM SO-DIMM

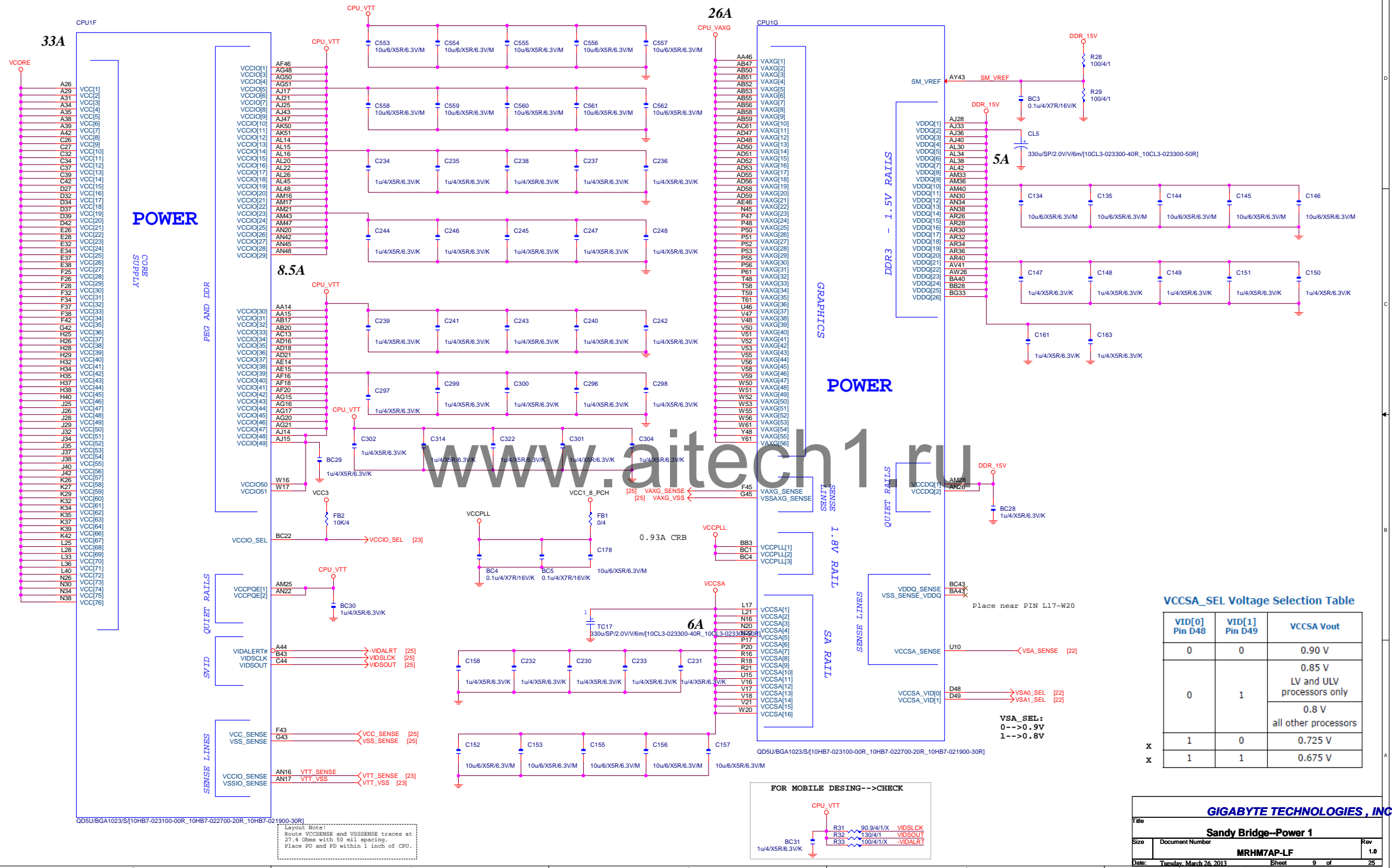
## DDR3 SDRAM SO-DIMM

## DDR3 SDRAM SO-DIMM

## DDR3 SDRAM SO-DIMM

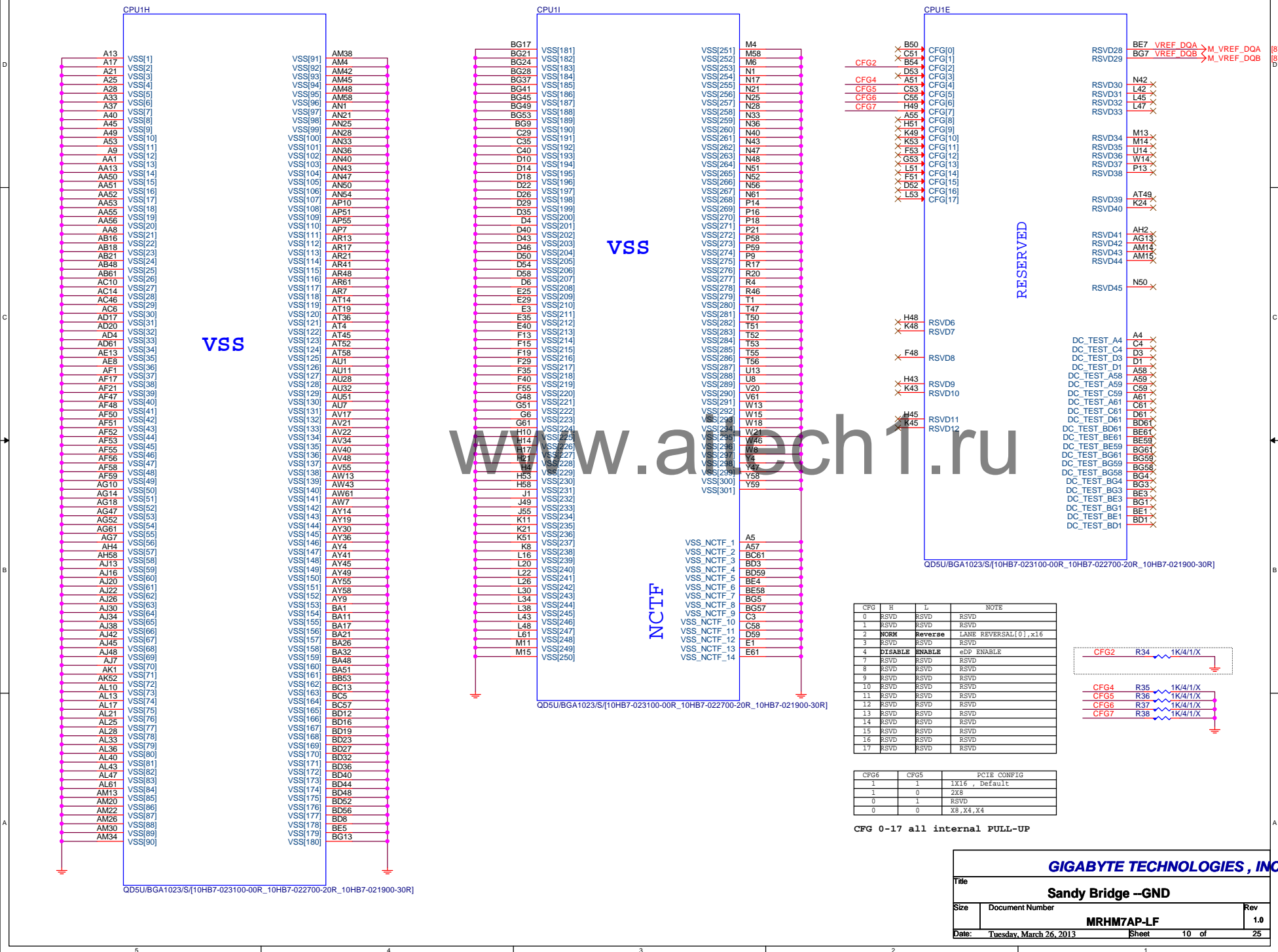


# Sandy Bridge 2C BGA Processor (Power)

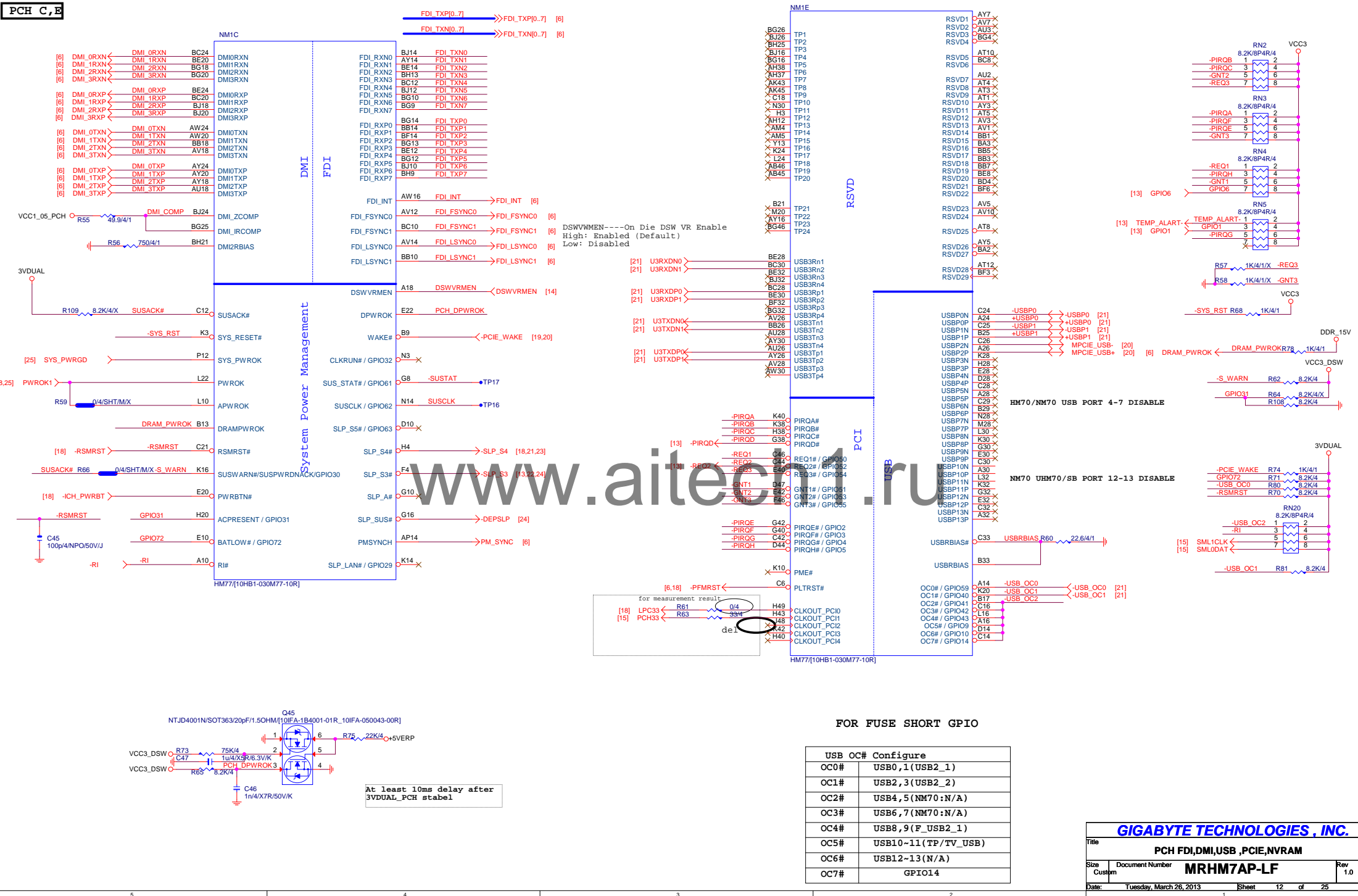


## Sandy Bridge 2C BGA Processor (GND)

## Sandy Bridge 2C BGA Processor (Reserved)





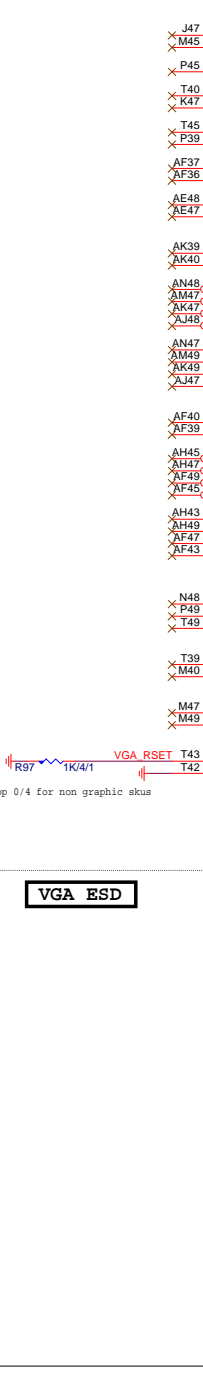


~~J47~~  
~~M45~~  
~~P45~~  
~~T40~~  
~~K47~~  
~~T45~~  
~~P39~~  
~~AF37~~  
~~AF36~~  
~~AE48~~  
~~AE47~~  
~~AK39~~  
~~AK40~~  
~~AN48~~  
~~AM47~~  
~~AK47~~  
~~LA48~~  
~~AN47~~  
~~AM49~~  
~~AK49~~  
~~AJ47~~  
~~AF40~~  
~~AF39~~  
~~AH45~~  
~~AH47~~  
~~AF49~~  
~~AF45~~  
~~AH43~~  
~~AH49~~  
~~AF47~~  
~~AF43~~  
~~N48~~  
~~P49~~  
~~T49~~  
~~T39~~  
~~M40~~  
~~M47~~  
~~M49~~  
~~R97~~

R97  1K4/1  VGA RSET  T43  
 T42 

up 0/4 for non graphic skus

VGA ESD



pull down?

[20] GPIO12

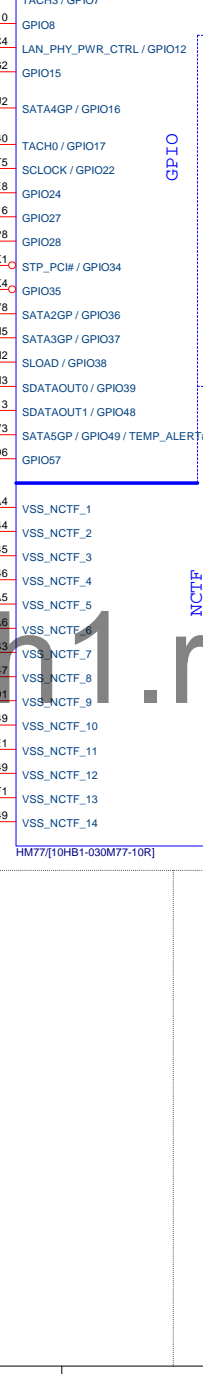
GP28:Lo disable VRM  
Hi enable VRM  
INTERNAL HIGH

[15] GPIO34

[14] GPIO48

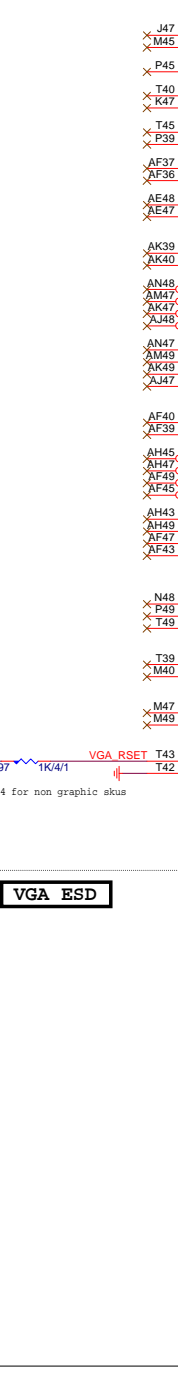
[12] TEMP\_ALARM

TP14

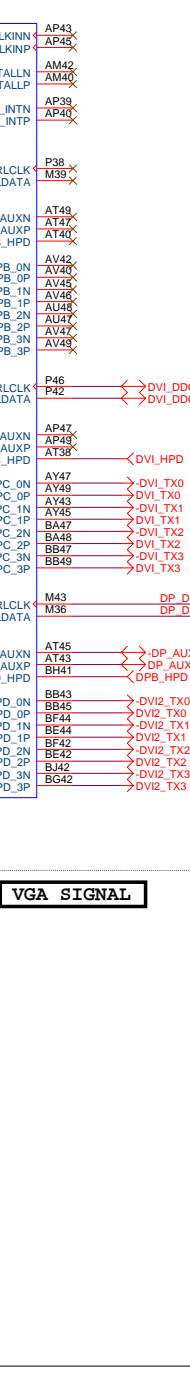


~~J47~~  
~~M45~~  
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~~T49~~  
~~T39~~  
~~M40~~  
~~M47~~  
~~M49~~  
 37  1K4/1 VGA RSET ~~T43~~  
 ~~T42~~  
 4 for non graphic akus

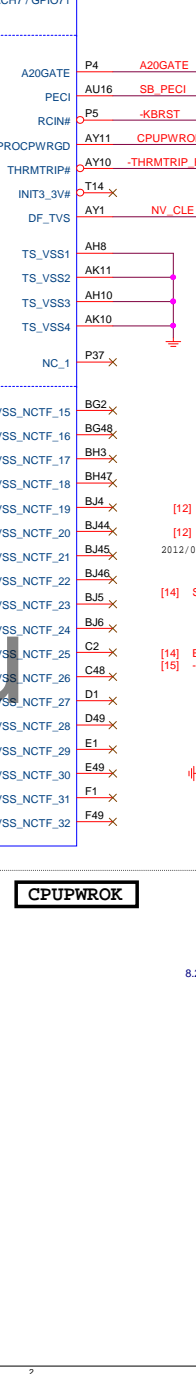
VGA ESD



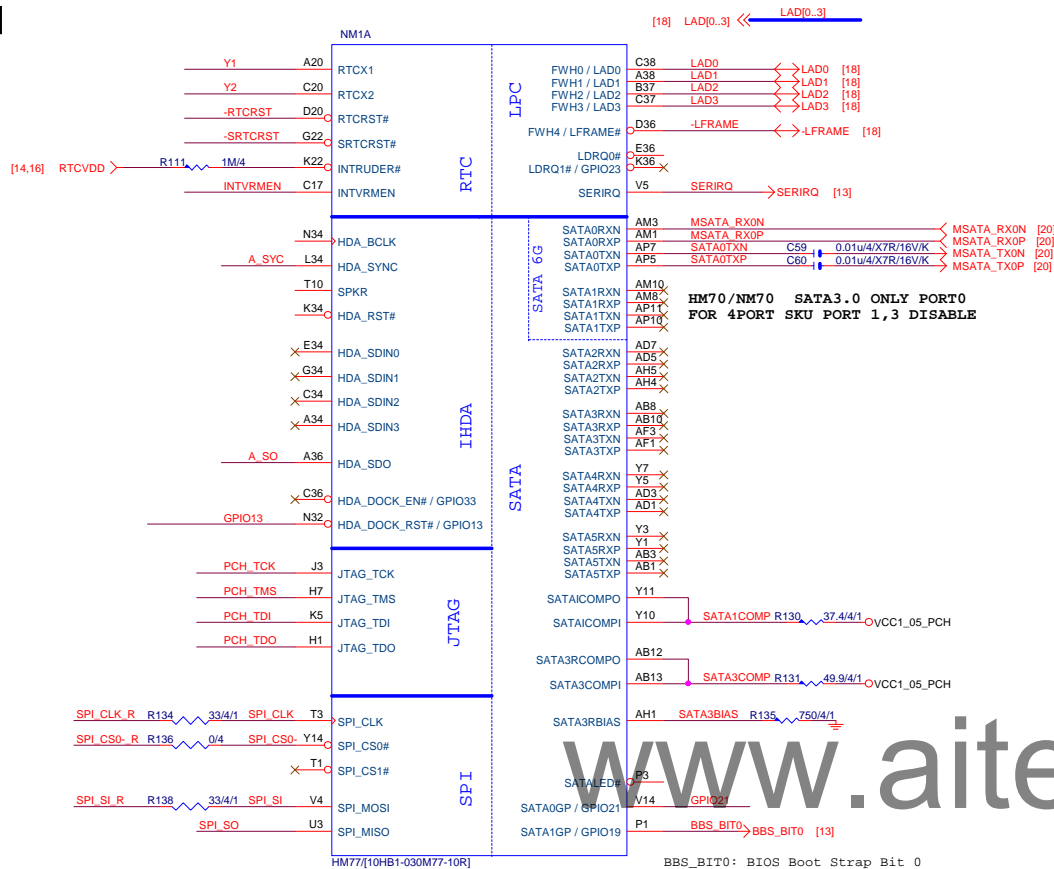
Chip	Pin	Signal	Notes
AP43	AP43	AP43	
	AP45	AP45	
	AM42	AM42	
	AM40	AM40	
	AP39	AP39	
	AP40	AP40	
	P38	P38	
	M35	M35	
	AT48	AT48	
	AT47	AT47	
AP47	AP47	AP47	
	AP48	AP48	
	AT38	AT38	
	AY47	AY47	
	AY49	AY49	
	AY45	AY45	
	BA47	BA47	
	BA48	BA48	
	BB47	BB47	
	BB49	BB49	
M43	M43	M43	
	M36	M36	
	AT45	AT45	
	AT43	AT43	
	BH41	BH41	
	BB43	BB43	
	BB45	BB45	
	BF44	BF44	
	BF42	BF42	
	BJ42	BJ42	
BG42	BG42	BG42	
	DP1	DP1	
	DP2	DP2	
	DP3	DP3	
	DP4	DP4	
	DP5	DP5	
	DP6	DP6	
	DP7	DP7	
	DP8	DP8	
	DP9	DP9	



A20GATE P4 A20GATE  
 PEGI AU16 SB PEGI  
 RCIN# P5 -KBRST  
 PROCPUWRGD AY11 CPUPWROK  
 THRMTRIP# AY10 -THRMTRIP#  
 INIT3\_3V# T14 X  
 DF\_TVS AY1 NV\_CLE  
 TS\_VSS1 AH8  
 TS\_VSS2 AK11  
 TS\_VSS3 AH10  
 TS\_VSS4 AK10  
 NC\_1 P37 X  
 SS\_NCTF\_15 BG2 X  
 SS\_NCTF\_16 BG48 X  
 SS\_NCTF\_17 BH3 X  
 SS\_NCTF\_18 BH47 X  
 SS\_NCTF\_19 BJ4 X [12]  
 SS\_NCTF\_20 BJ44 X [12]  
 SS\_NCTF\_21 BJ45 2012/0  
 SS\_NCTF\_22 BJ46 X  
 SS\_NCTF\_23 BJ5 X [14]  
 SS\_NCTF\_24 BJ6 X  
 SS\_NCTF\_25 C2 X [14]  
 SS\_NCTF\_26 C48 X [15]  
 SS\_NCTF\_27 D1 X  
 SS\_NCTF\_28 D49 X  
 SS\_NCTF\_29 E1 X  
 SS\_NCTF\_30 E49 X  
 SS\_NCTF\_31 F1 X  
 SS\_NCTF\_32 F49 X  
 CPUPWROK  
 8.



## PCH A

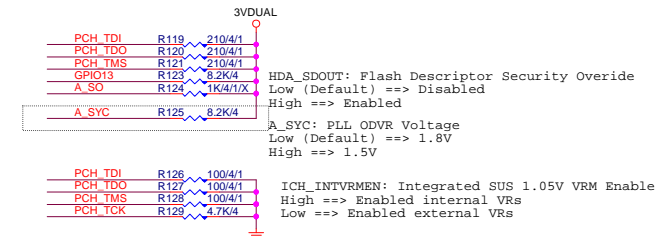
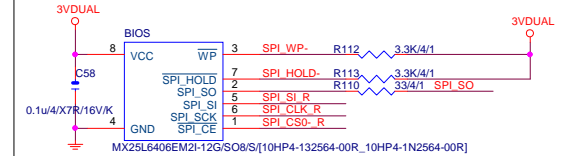


## PCH HS

Boot BIOS Strap		
PCI GNT#1	BBS_BIT0	Boot BIOS Location
1	1	SPI (Default)
0	1	Reserved (NAND)
0	0	LPC

1 means floating  
0 means PD 1k

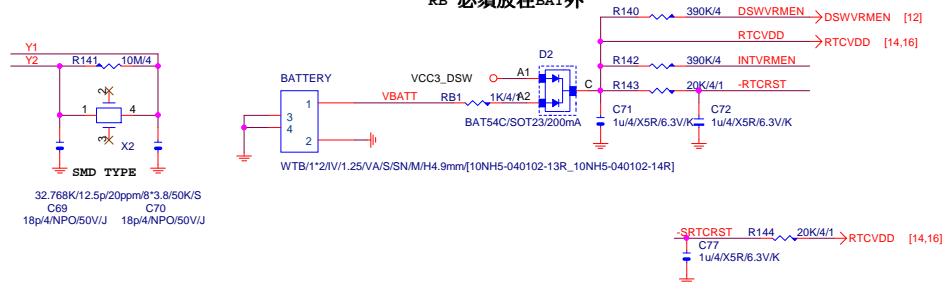
## BIOS



BATTERY

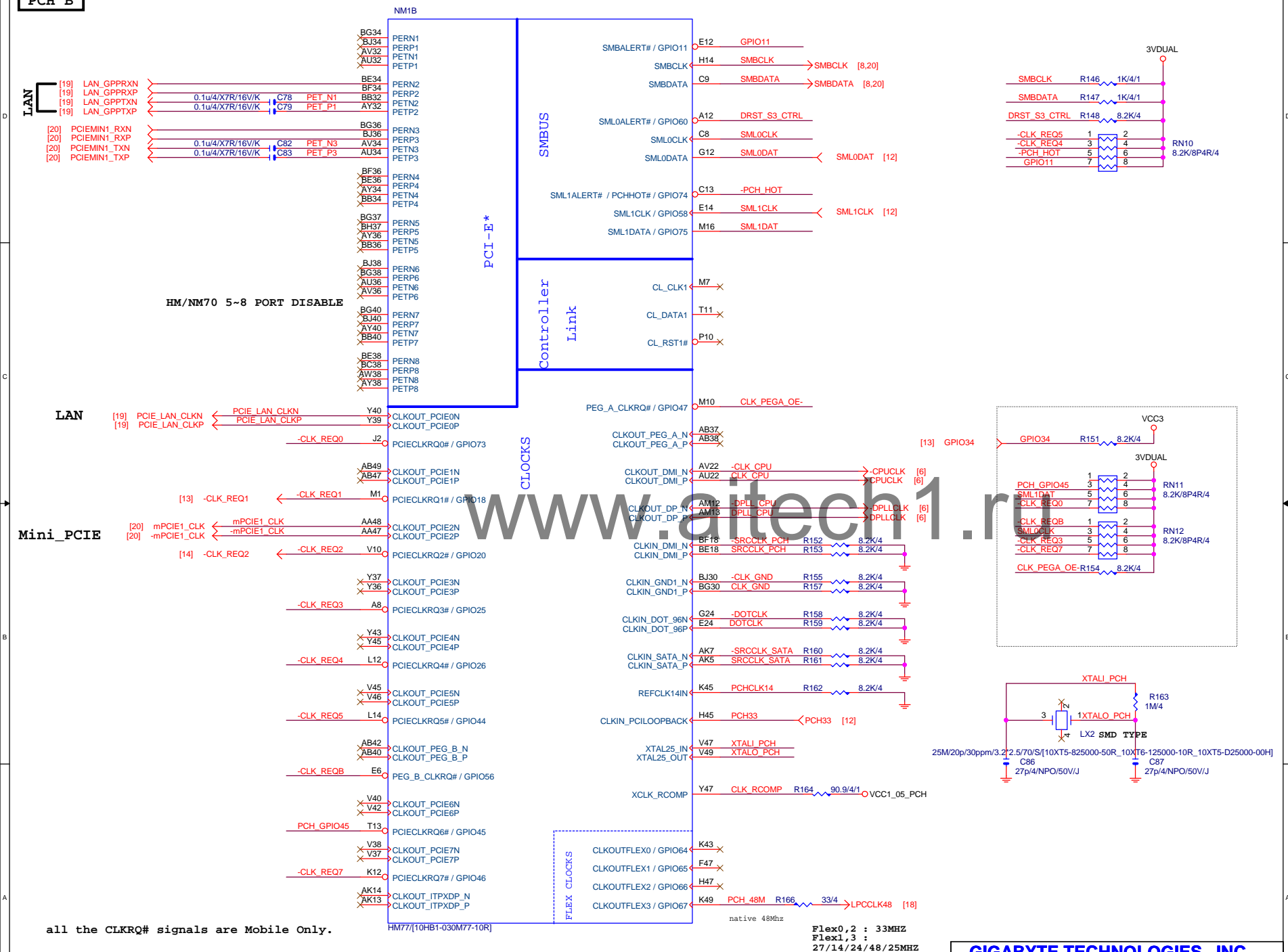
CR2032[11BL5-032032-31R\_11BL5-032032-32R]

RB 必須放在BAT外



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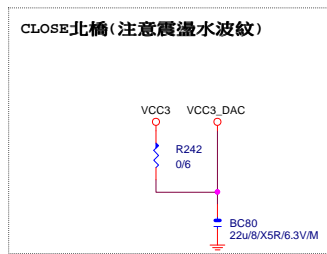
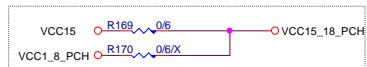
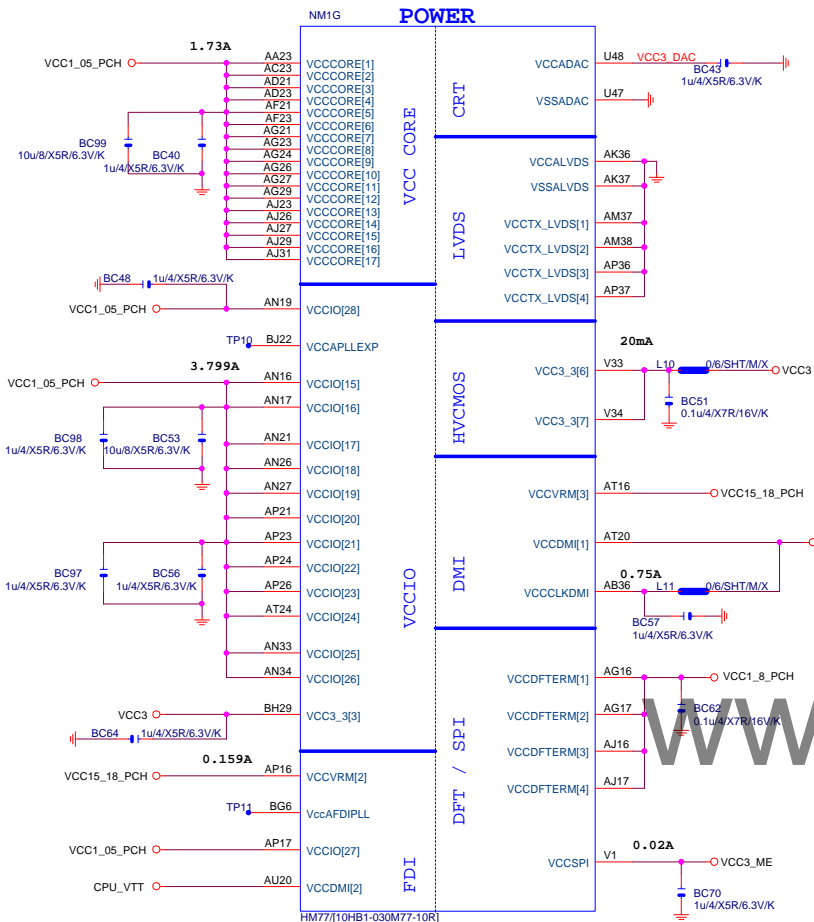
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PCH HOST , SATA, PCI		
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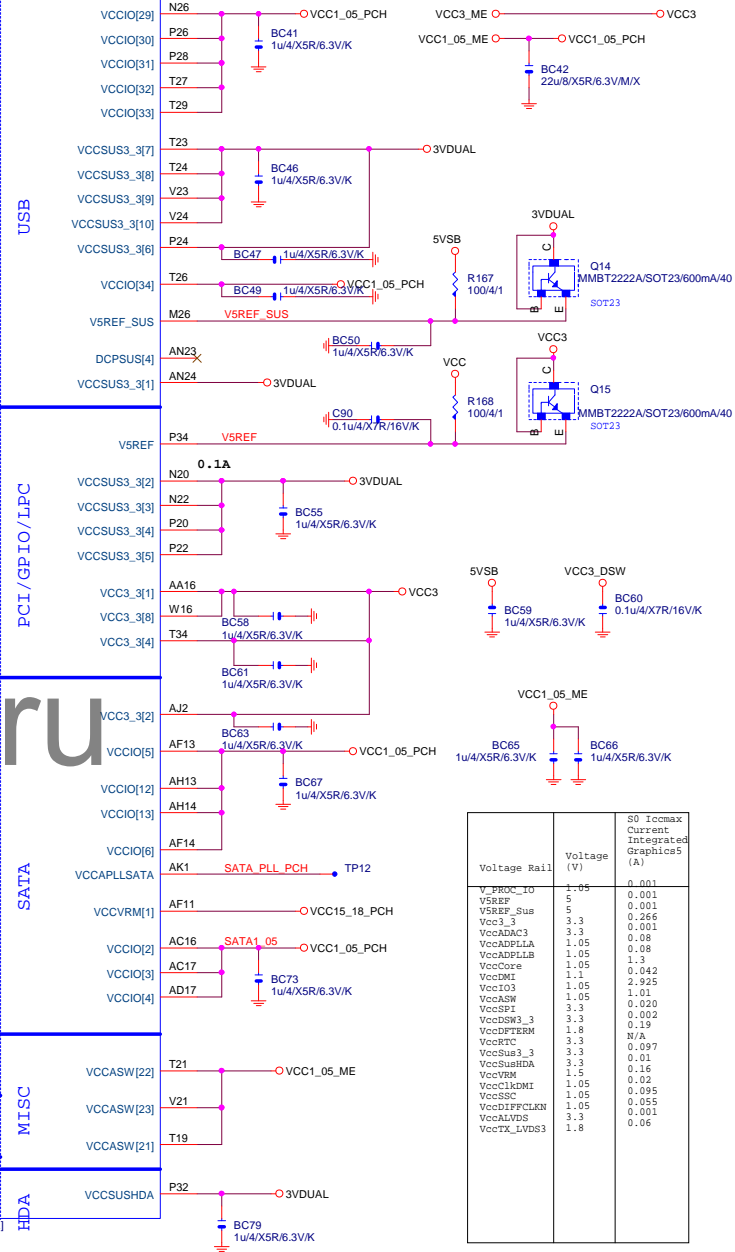
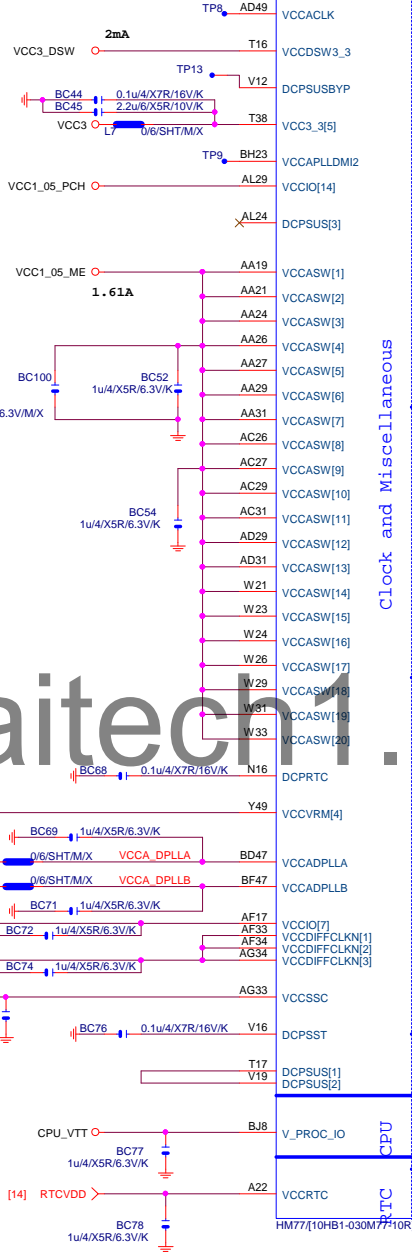
## GIGABYTE TECHNOLOGIES, INC.

Title			PCH GPIO , CTRL , AUDIO
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PCH G,J POWER



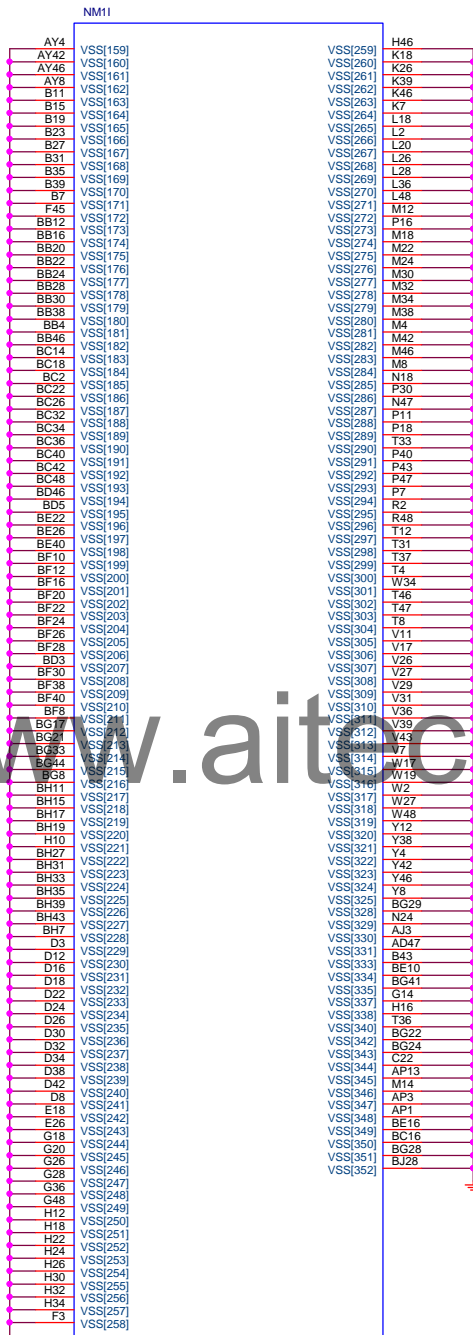
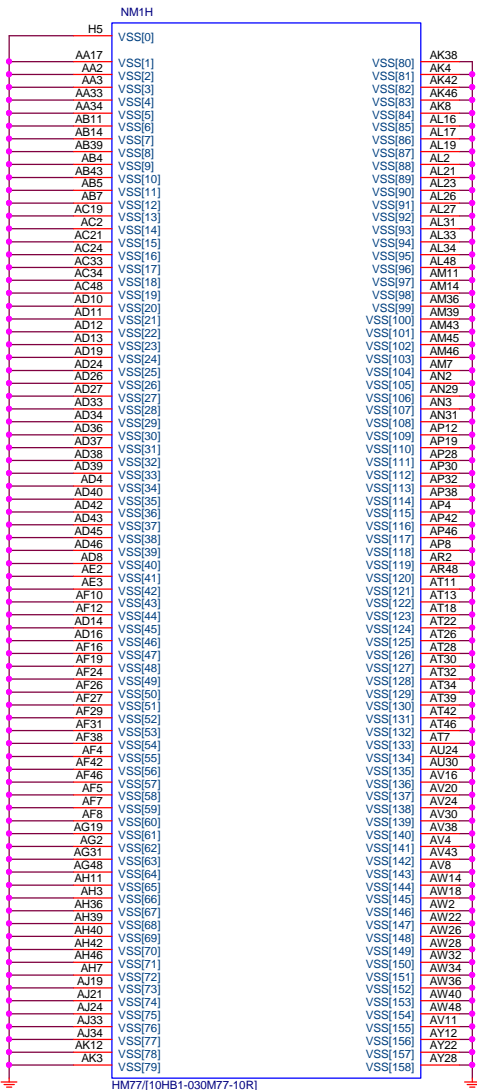
```
CougarPoint Total PWR Consumption:
1.05V => 5.608A
5V => 0.002A
3.3V => 0.399A
1.8V => 0.25A
1.5V => 0.16A
```



Voltage Rail	Voltage (V)	Current Integrated Graphics (A)	50 Items Current
V_PROC_IO	1.05	0.001	
VSRF	5	0.001	
VSRF_Sus	5	0.001	
Vcc3_3	3.3	0.001	
VccADAC3	3.3	0.001	
VccADPLL4	1.05	0.08	
VccADPLL8	1.05	0.08	
VccCore	1.05	1.3	0.042
VccDMI	1.1	2.925	
VccIO3	1.05	1.01	0.020
VccSW	1.05	0.020	
VccDSW3_3	3.3	0.002	
VccDPTHERM	1.8	0.19	
VccRTC	3.3	W/A	0.097
VccUSB3_3	3.3	0.01	
VccSUBHDA	3.3	0.16	
VccVRM	1.05	0.02	
VccVDDCLKN1	1.05	0.095	
VccSSC	1.05	0.095	
VccDIFFCLKIN	1.05	0.051	
VccALVDS	3.3	0.001	
VccCTV_LVDS3	1.8	0.06	

**GIGABYTE TECHNOLOGIES, INC.**

<b>GIGABYTE TECHNOLOGIES ,</b>			
Title			
<b>PCH PWR ,GND</b>			
Size	Document Number	Rev	
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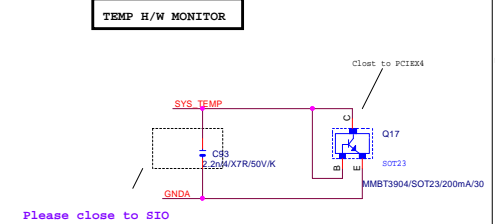
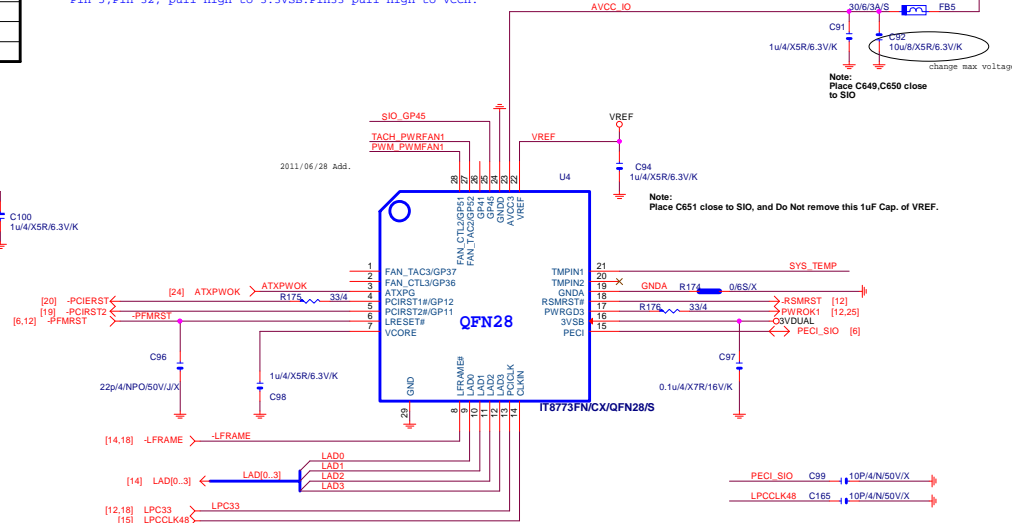
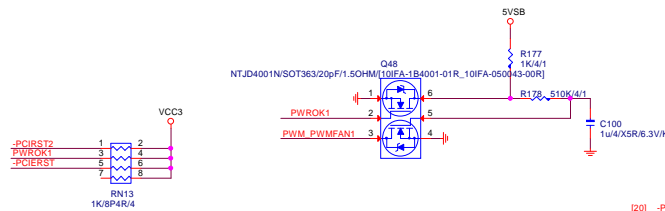
# Power On Strapping Options

Symbol	value	Description
JP4		
Pin 126	K8PWR_EN	1 K8 power sequence function is disabled
		0 K8 power sequence function is enabled
		11 The default value of EC Index 15h/16h/17h is 80h
JP3 & JP5		
Pin 124 & 46	FAN_CTL_SEL	10 The default value of EC Index 15h/16h/17h is FFh(Fan off)
		01 The default value of EC Index 15h/16h/17h is 00h(Fan full speed)
		00 The default value of EC Index 15h/16h/17h is 40h
JP2		
Pin122	WDT_EN	1 Disable WDT to rest PWROK
		0 Enable WDT to rest PWROK

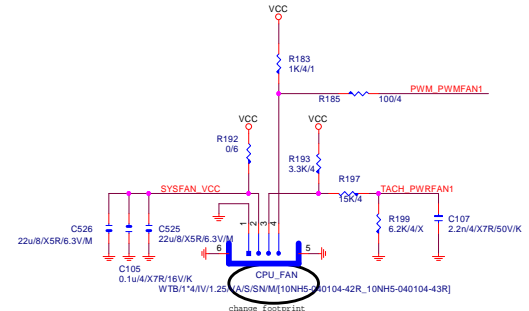
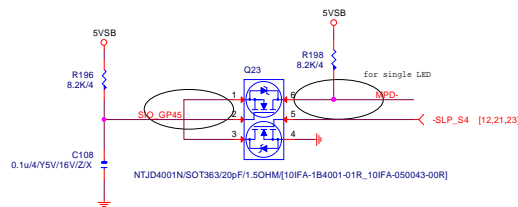
If without use these pins, Please pull-up. Don't let it floating

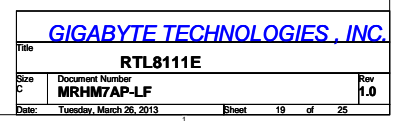
- 1.Pin 6:ATXPG
- 2.Pin 29:SYS##
- 3.Pin 21/ Pin 57/ Pin 59/ Pin61
- 4.Pin37-40 KCLK/KDAT/MCLK/MDAT
- 5.Pin 63 pull high to 3VSB

Note:use EUP function:Pin29/Pin30/Pin31/Pin34/Pin42 pull high to SYS\_3VSB.  
Pin 5,Pin 32, pull high to 3.VSB.Pin33 pull high to VCCH.

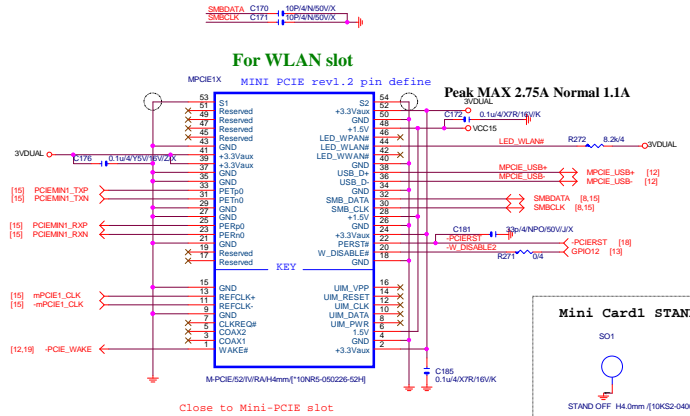


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**MINI\_PCIE**

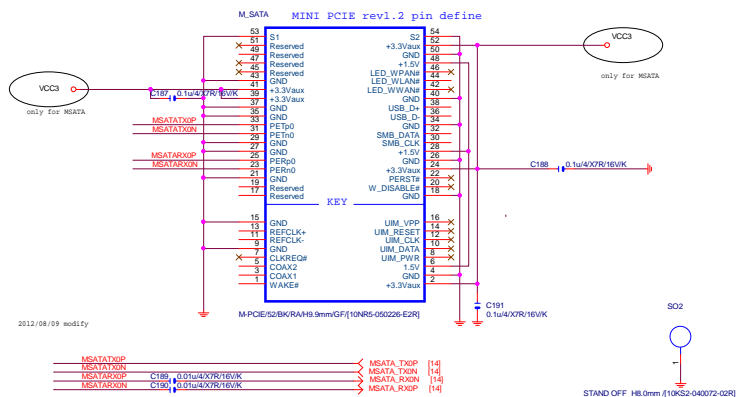


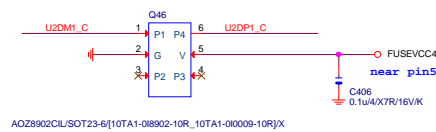
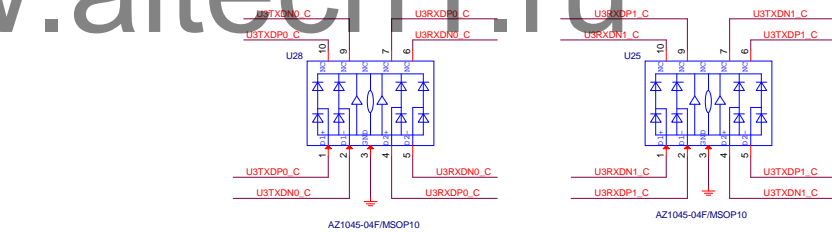
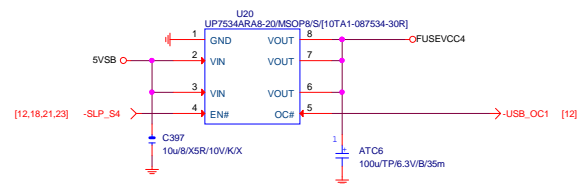
**MSATA**

## EXT\_CON PWR CIRCUIT

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**For mSATA slot**





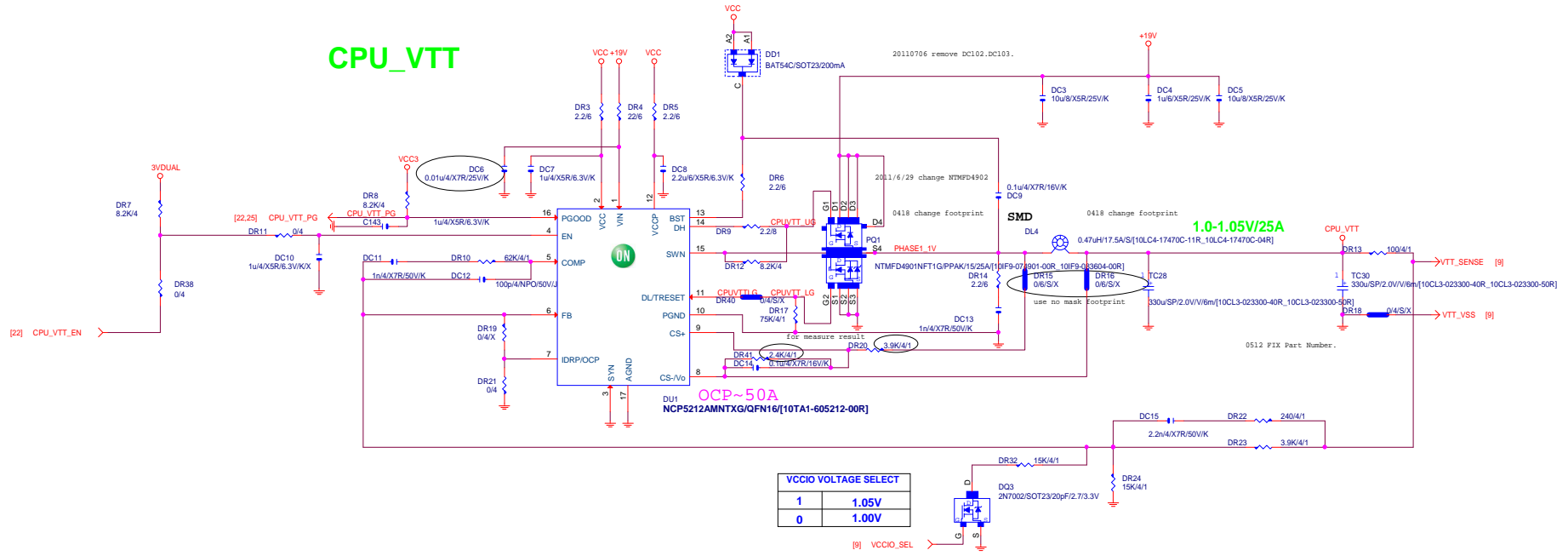
**VCCSA**

VCCSA_SEL0	VCCSA_SEL1	Selected VCCSA (VvL)	
0	0	0.9V	SV
0	1	0.85V	
1	0	0.775V	using 0.8V
1	1	0.75V	using 0.8V

The schematic diagram illustrates the Non ME board's internal components and connections. Key elements include:

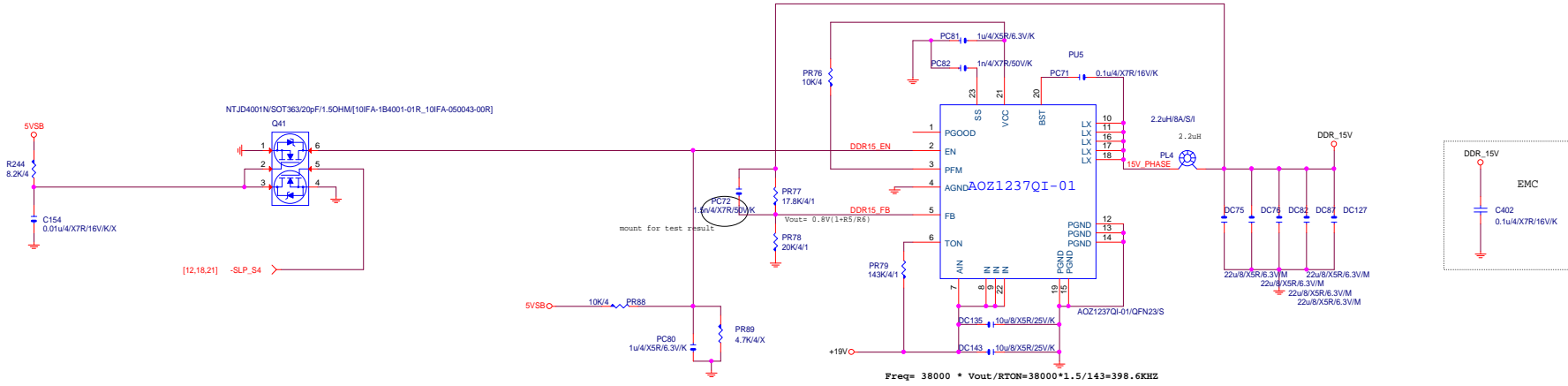
- Power Regulation:** A 3V DUAL regulator (DR1, 8.2K/4/1) provides VCC1\_05\_EN to the CPU (Q33).
- Memory:** A 1GB DDR2 module (NTJD4001N/SOT36320P/F1.50MH[10IFA-184001-01R\_10IFA-050043-00R]) is connected to the CPU's memory pins.
- Storage:** A 16GB NAND flash (BC96, 10u8/XSR/6.3V/K) is connected to the CPU's storage pins.
- Connectors:** The board features a 3.16K/4/1 connector (R764) and a 10K/4/1 connector (R766).
- Other Components:** Various capacitors (C548, C547, C133, TC16) and resistors (R765, R771, R772) are used for signal conditioning and power filtering.

The diagram also shows the CPU's internal logic, including the CPU\_VTT\_EN signal and the CPU\_VTT\_EN pin (22,23).

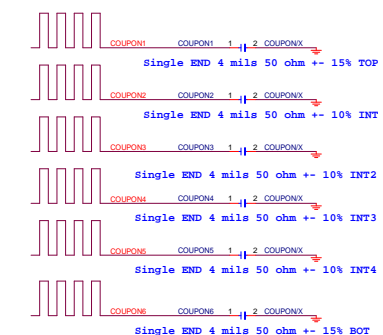


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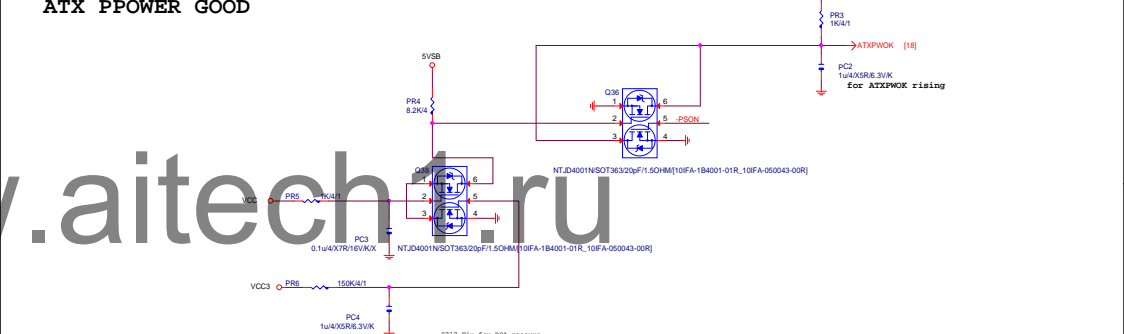
**DDR15V**  
11.21A



FOR INOUT AND PROTECT CIRCUIT



ATX PPOWER GOOD



**3VUDAL**  
Voltage level : 3.3V  
Max current : 13A

